FAIRCHILD SEMICONDUCTOR®

October 2008

FAN2106 — TinyBuck™
6A, 24V Input, Integrated Synchronous Buck Regulator

Features

- 6A Output Current
- Over 95% Efficiency
- Fully Synchronous Operation with Integrated Schottky Diode on Low-side MOSFET Boosts Efficiency
- Programmable Frequency Operation: 200KHz to 600KHz
- Power-good Signal
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Wide Input Range: 3V to 24V
- Output Voltage Range: 0.8V to 90% V_{IN}
- Input Under-Voltage Lockout
- Programmable Current Limit
- Under-Voltage, Over-Voltage, and Thermal Protections
- 5x6mm, 25-pin, 3-pad MLP

Applications

- Graphics Cards
- Battery-powered Equipment
- Set-top Boxes
- Point-of-load Regulation
- Servers

Description

The FAN2106 TinyBuck™ is an easy-to-use, cost and space-efficient, 6A synchronous buck solution. It enables designers to solve high current requirements in a small area with minimal external components.

External compensation, programmable switching frequency, and current limit features allow for design optimization and flexibility.

The summing current mode modulator uses lossless current sensing for current feedback and over-current, and includes voltage feedforward.

Fairchild's advanced BiCMOS power process combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package provide the ability to dissipate high power in a small package.

Output over voltage, under voltage, and thermal shutdown protections help protect the device from damage during fault conditions.

Related Application Notes

- *AN-6033 — FAN2106 Design Guide*

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
FAN2106MPX	-10°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Green	Tape and Reel
FAN2106EMPX	-40°C to 85°C	Molded Leadless Package (MLP) 5x6mm	Green	Tape and Reel

For Fairchild's definition of "green" please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Diagram

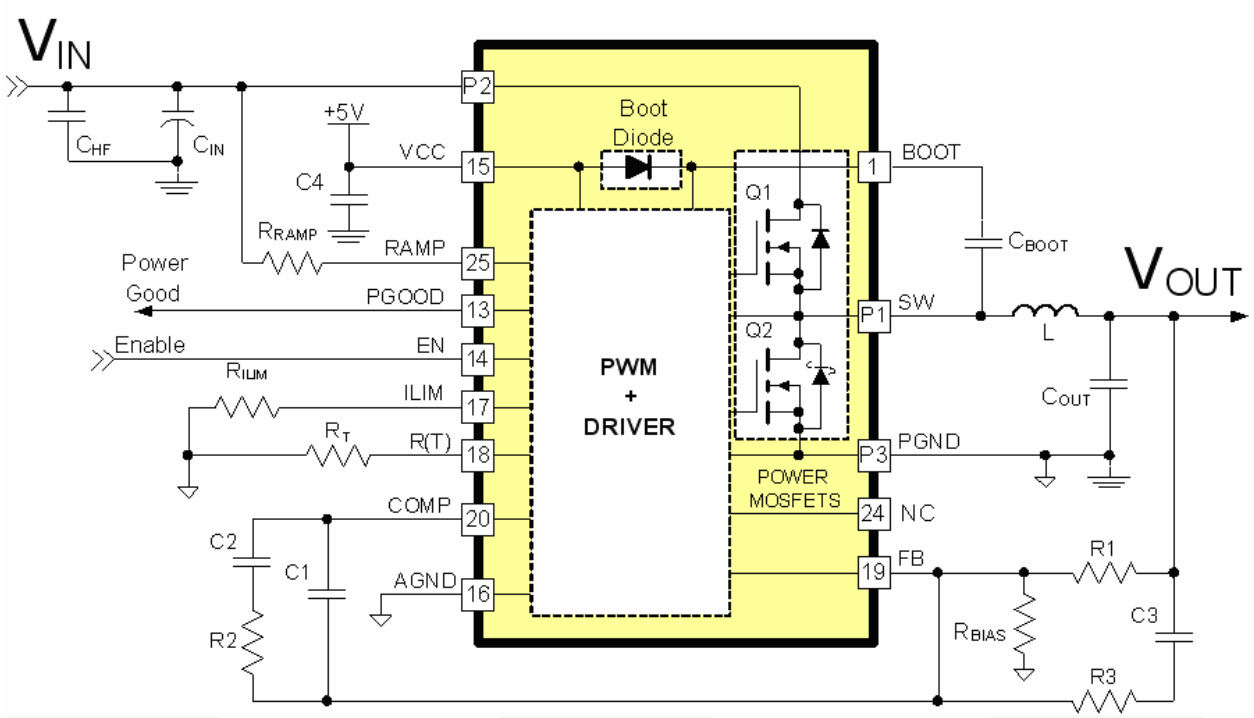

Figure 1. Typical Application

Block Diagram

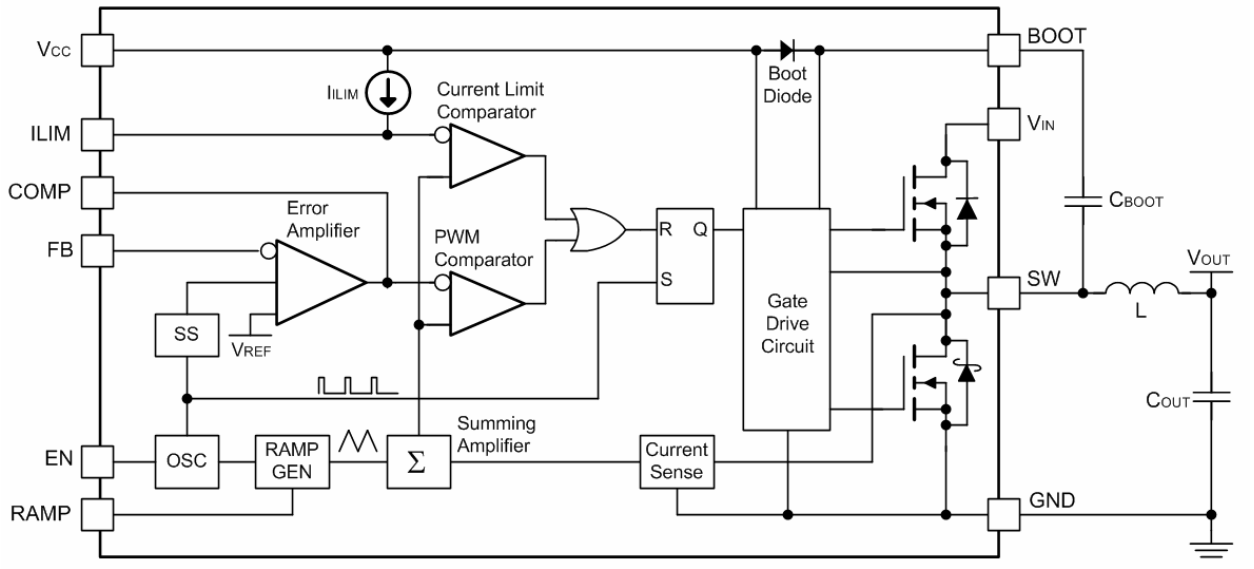

Figure 2. Block Diagram

Pin Configuration

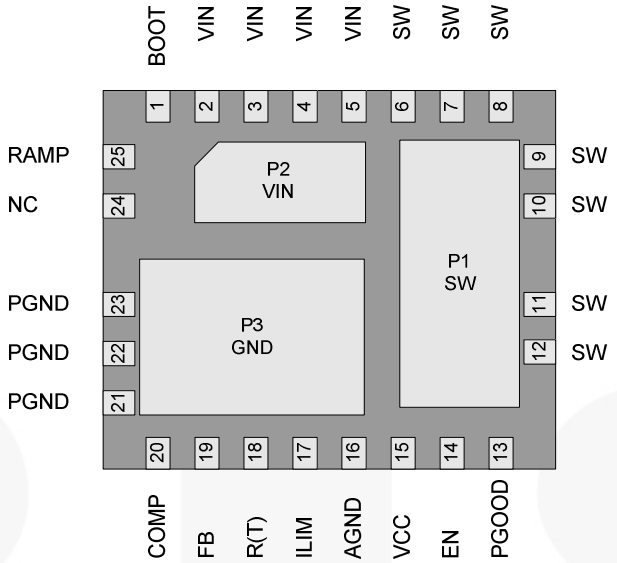

Figure 3. MLP 5x6mm Pin Configuration (Bottom View)

Pin Definitions

Pin #	Name	Description
P1, 6-12	SW	**Switching Node**.
P2, 2-5	VIN	**Power Input Voltage**. Connect to the main input power source.
P3, 21-23	PGND	**Power Ground**. Power return and Q2 source.
1	BOOT	**High-Side Drive BOOT Voltage**. Connect through capacitor (C_{BOOT}) to SW. The IC includes an internal synchronous bootstrap diode to recharge the capacitor on this pin to V_{CC} when SW is LOW.
13	PGOOD	**Power-Good Flag**. An open-drain output that pulls LOW when FB is outside a ±10% range of the reference. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	**ENABLE**. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched fault condition. This input has an internal pull-up when the IC is functioning normally. When a latched fault occurs, EN is discharged by a current sink.
15	VCC	**Input Bias Supply for IC**. The IC's logic and analog circuitry are powered from this pin.
16	AGND	**Analog Ground**. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	**Current Limit**. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the default setting.
18	R(T)	**Oscillator Frequency**. A resistor (R_T) from this pin to AGND sets the PWM switching frequency.
19	FB	**Output Voltage Feedback**. Connect through a resistor divider to the output voltage.
20	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and FB.
24	NC	**No Connect**. This pin is not used.
25	RAMP	**Ramp Amplitude**. A resistor (R_{RAMP}) connected from this pin to VIN sets the ramp amplitude and provides voltage feedforward functionality.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Unit
VIN to PGND			28	V
VCC to AGND	AGND = PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.3	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20ns, f ≤ 600KHz)	-5	30	V
All other pins		-0.3	V_{CC}+0.3	V
ESD	Human Body Model, JEDEC JESD22-A114	2.0		kV
	Charged Device Model, JEDEC JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Bias Voltage	VCC to AGND	4.5	5.0	5.5	V
V_{IN}	Supply Voltage	VIN to PGND	3		24	V
T_A	Ambient Temperature	FAN2106M	-10		+85	°C
		FAN2106EM	-40		+85	°C
T_J	Junction Temperature				+125	°C

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_{STG}	Storage Temperature		-65		+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+300	°C
T_{VP}	Vapor Phase, 60 Seconds				+215	°C
T_I	Infrared, 15 Seconds				+220	°C
θ_{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
$\theta_{J\text{-}PCB}$	Thermal Resistance: Junction-to-Mounting Surface			35[1]		°C/W
P_D	Power Dissipation, T_A = 25°C				2.8[1]	W

Note:

1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 25. Actual results are dependent on mounting method and surface related to the design.

Electrical Specifications

Recommended operating conditions are the result of using the circuit shown in Figure 1 unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies					
V_{CC} Current	SW = Open, FB = 0.7V, V_{CC} = 5V, f_{SW} = 600KHz		8	12	mA
	Shutdown: EN = 0, V_{CC} = 5V		7	10	µA
V_{CC} UVLO Threshold	Rising V_{CC}	4.1	4.3	4.5	V
	Hysteresis		300		mV
Oscillator					
Frequency	R_T = 50KΩ	255	300	345	KHz
	R_T = 24KΩ	540	600	660	KHz
Minimum On-Time(2)			50	65	ns
Ramp Amplitude, pk–pk	16V_{IN}, 1.8V_{OUT}, R_T = 30KΩ, R_{RAMP} = 200KΩ		0.53		V
Minimum Off-Time(2)			100	150	ns
Reference					
Reference Voltage (V_{FB})	FAN2106M, 25°C	794	800	806	mV
(See Figure 4 for Temperature Coefficient)	FAN2106EM, 25°C	795	800	805	mV
Error Amplifier					
DC Gain(2)	V_{CC} = 5V	80	85		dB
Gain Bandwidth Product(2)		12	15		MHz
Output Voltage (V_{COMP})		0.4		3.2	V
Output Current, Sourcing	V_{CC} = 5V, V_{COMP} = 2.2V	1.5	2.2		mA
Output Current, Sinking	V_{CC} = 5V, V_{COMP} = 1.2V	0.8	1.2		mA
FB Bias Current	V_{FB} = 0.8V, 25°C	-850	-650	-450	nA
Protection and Shutdown					
Current Limit	R_{ILIM} Open	6	8	10	A
I_{LIM} Current		-11	-10	-9	µA
Over-Temperature Shutdown	Internal IC Temperature		+155		°C
Over-Temperature Hysteresis			+30		°C
Over-Voltage Threshold	2 Consecutive Clock Cycles	110	115	120	%V_{OUT}
Under-Voltage Shutdown	16 Consecutive Clock Cycles	68	73	78	%V_{OUT}
Fault Discharge Threshold	Measured at FB Pin		250		mV
Fault Discharge Hysteresis	Measured at FB Pin (V_{FB} ~500mV)		250		mV
Soft-Start					
V_{OUT} to Regulation (T0.8)	Frequency = 600KHz		5.3		ms
Fault Enable/SSOK (T1.0)			6.7		ms

Note:

2. Specifications guaranteed by design and characterization; not production tested.

Electrical Specifications (Continued)

Recommended operating conditions are the result of using the circuit shown in Figure 1 unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Control Functions					
EN Threshold, Rising			1.35	2.00	V
EN Hysteresis			250		mV
EN Pull-Up Resistance			800		KΩ
EN Discharge Current	Auto-restart mode		1		µA
FB OK Drive Resistance				800	Ω
PGOOD Threshold (Compared to V_{REF})	FB < V_{REF}	-14	-11	-8	%V_{REF}
	FB > V_{REF}	+7	+10	+13	%V_{REF}
PGOOD Output Low	$I_{OUT} \leq$ 2mA			0.4	V

Typical Characteristics

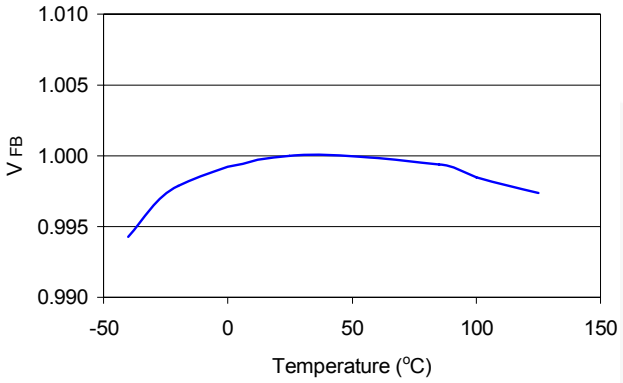

Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

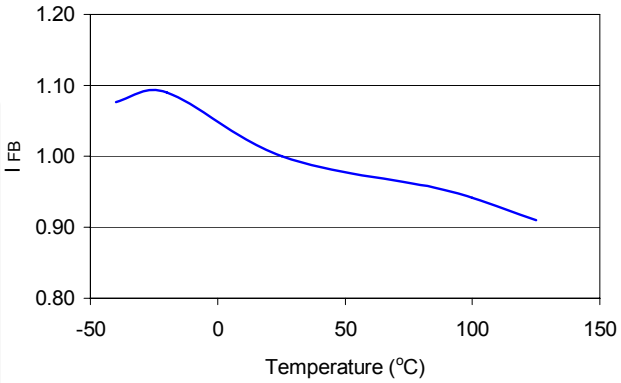

Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

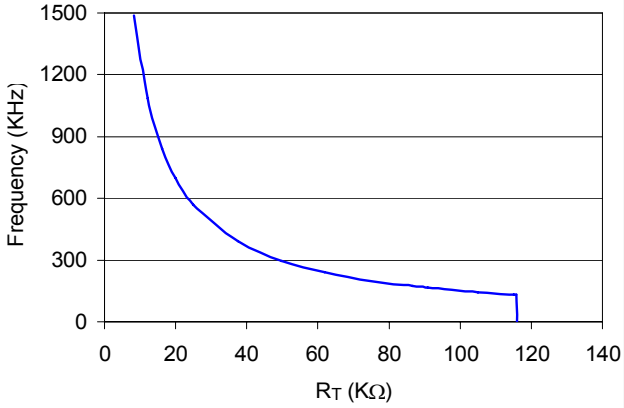

Figure 6. Frequency vs. R_T

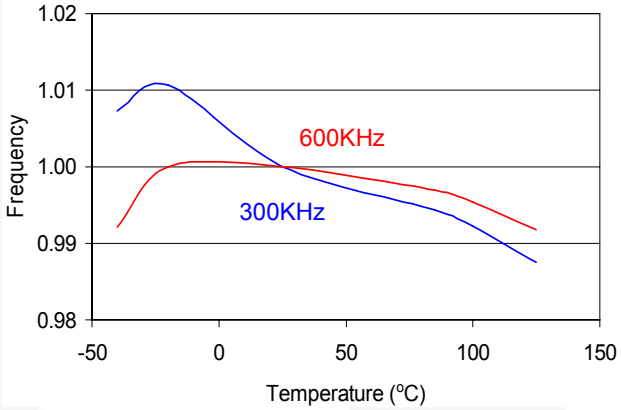

Figure 7. Frequency vs. Temperature, Normalized

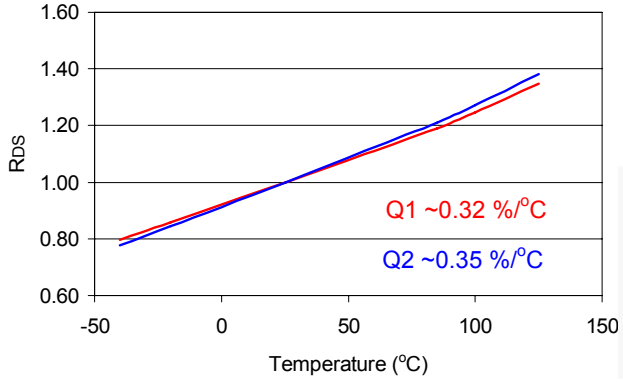

Figure 8. R_{DS} vs. Temperature, Normalized (V_{CC} = V_{GS} = 5V)

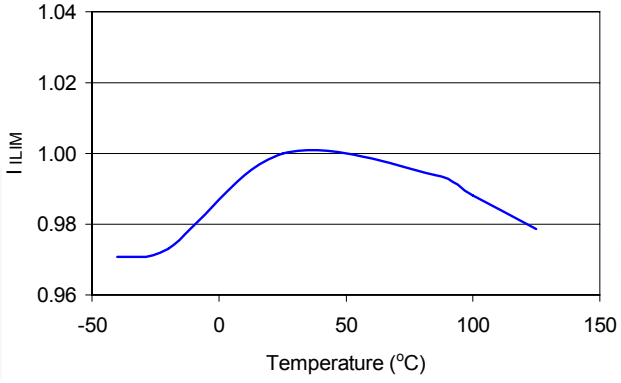

Figure 9. ILIM Current (I_{ILIM}) vs. Temperature, Normalized

Application Circuit

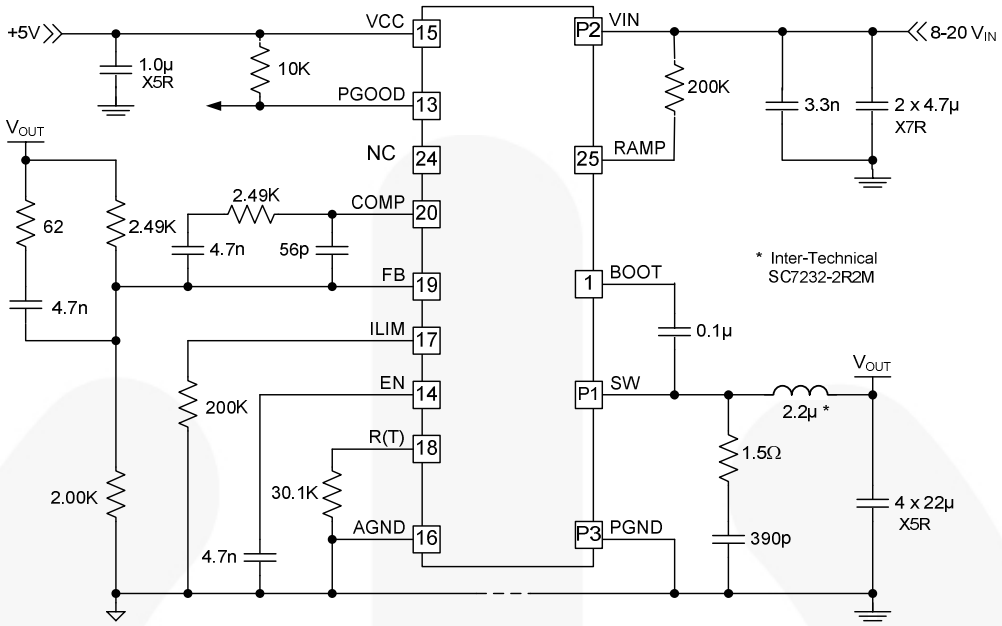

Figure 10. Application Circuit: 1.8V_{OUT}, 500KHz

Typical Performance Characteristics

Typical operating characteristics using the circuit shown in Figure 10. V_{IN}=16V, V_{CC}=5V, unless otherwise specified.

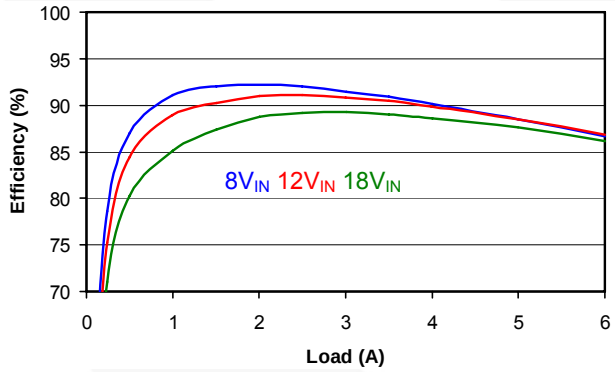

Figure 11. 1.8V_{OUT} Efficiency Over V_{IN} vs. Load

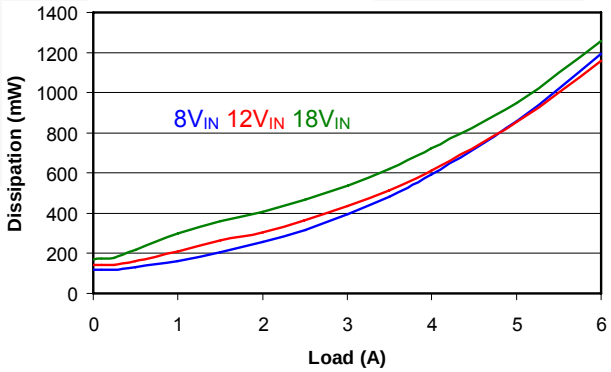

Figure 12. 1.8V_{OUT} Dissipation Over V_{IN} vs. Load

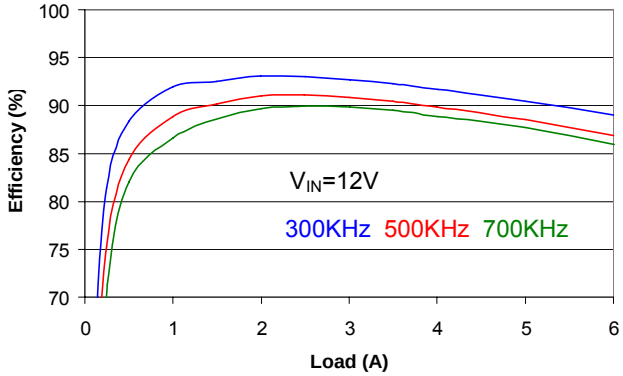

Figure 13. 1.8V_{OUT} Efficiency Over Frequency vs. Load (Circuit Value Changes)

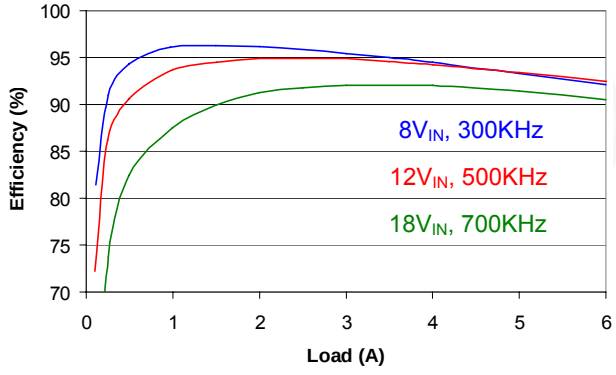

Figure 14. 3.3V_{OUT} Efficiency vs. Load (Circuit Value Changes)

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit shown in Figure 10. V_{IN}=16V, V_{CC}=5V, unless otherwise specified.

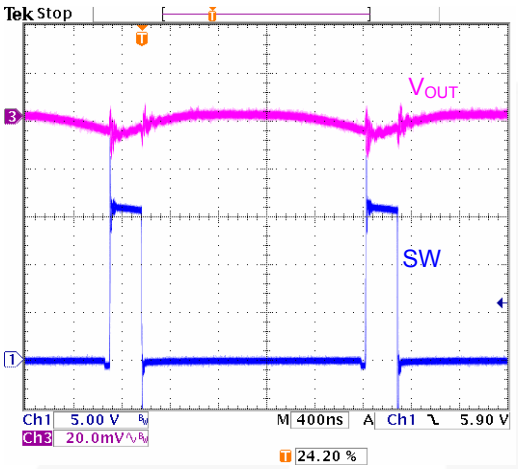

Figure 15. SW and V_{OUT} Ripple, 6A Load

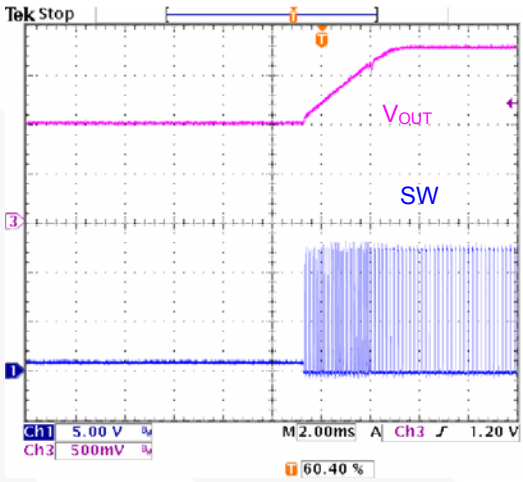

Figure 16. Startup with 1V Pre-Bias on V_{out}

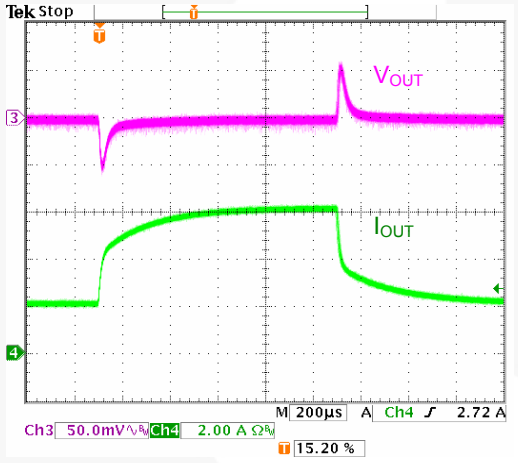

Figure 17. Transient Response, 2-6A Load

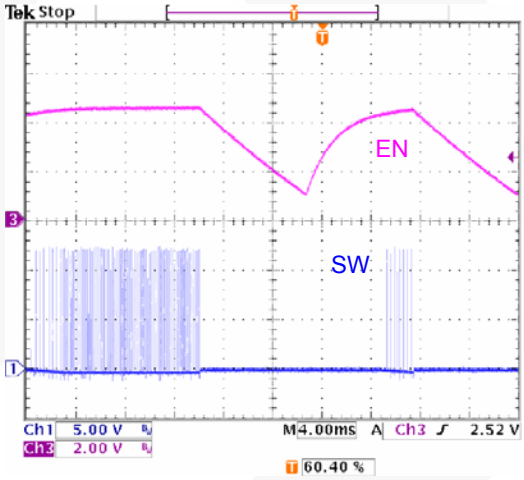

Figure 18. Re-start on Fault

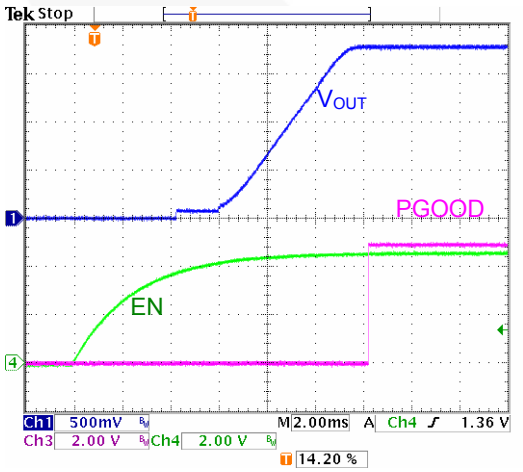

Figure 19. Startup, 3A Load

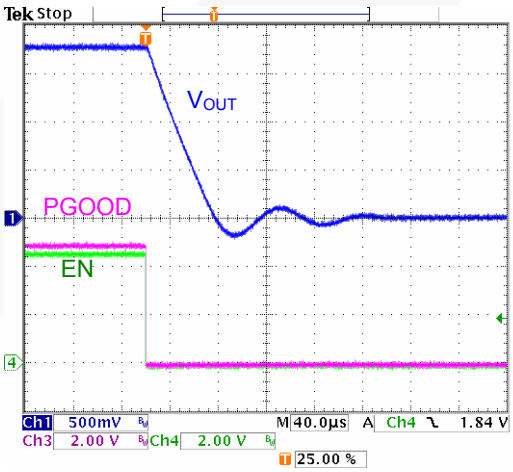

Figure 20. Shutdown, 3A Load

Circuit Description

Application Note *AN-6033 — FAN2106 Design Guide* includes a spreadsheet design aid to calculate external component values and verify loop stability given the following inputs:

- Output voltage
- Input voltage range
- Maximum output load current
- Maximum load transient current and maximum allowable output drop during load transient
- Maximum allowable output ripple
- Desired switching frequency

Download *AN-6033 — FAN2106 Design Guide* at:
http://www.fairchildsemi.com/an/AN/AN-6033.pdf

Initialization

Once V_{CC} exceeds the UVLO threshold and EN is HIGH, the IC checks for an open or shorted FB pin before releasing the internal soft-start ramp (SS).

If R1 is open (Figure 1), the error amplifier output (COMP) is forced LOW and no pulses are generated. After the SS ramp times out (T1.0), an under-voltage latched fault occurs.

If the parallel combination of R1 and R_{BIAS} is ≤ 1KΩ, the internal SS ramp is not released and the regulator does not start.

Soft-Start

Once internal SS ramp has charged to 0.8V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0V (T1.0), the “Fault Latch” is inhibited.

To avoid skipping the soft-start cycle, it is necessary to apply V_{IN} before V_{CC} reaches its UVLO threshold.

Soft-start time is a function of oscillator frequency.

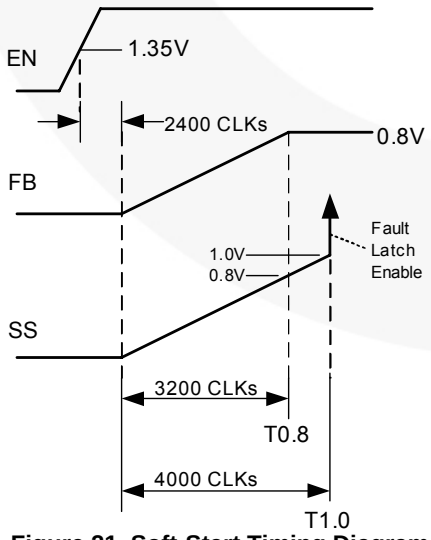

Figure 21. Soft-Start Timing Diagram

The regulator does not allow the low-side MOSFET to operate in full synchronous rectification mode until internal SS ramp reaches 95% of V_{REF} (~0.76V). This helps the regulator to start on a pre-biased output and ensures that inductor current does not "ratchet" up during the soft-start cycle.

V_{CC} UVLO or toggling the EN pin discharges the SS and resets the IC.

Bias Supply

The FAN2106 requires a 5V supply rail to bias the IC and provide gate-drive energy. Connect a ≥ 1.0µf X5R or X7R decoupling capacitor between VCC and PGND.

Since V_{CC} is used to drive the internal MOSFET gates, supply current is frequency and voltage dependent. Approximate V_{CC} current (I_{CC}) can be calculated using:

$$I_{CC(mA)} = 4.58 + [(\frac{V_{CC} - 5}{227} + 0.013) \bullet (f - 128)] \quad (1)$$

where frequency (f) is expressed in KHz.

Setting the Output Voltage

The output voltage of the regulator can be set from 0.8V to 80% of V_{IN} by an external resistor divider (R1 and R_{BIAS} in Figure 1).

The internal reference is 0.8V with 650nA, sourced from the FB pin to ensure that, if the pin is open, the regulator does not start.

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650nA \quad (2)$$

Connect R_{BIAS} between FB and AGND.

Setting the Frequency

Oscillator frequency is determined by an external resistor, R_T, connected between the R(T) pin and AGND:

$$f_{(KHz)} = \frac{10^6}{(65 \bullet R_T) + 135} \quad (3)$$

where R_T is expressed in KΩ.

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \quad (4)$$

where frequency (f) is expressed in KHz.

The regulator can not start if R_T is left open.

Calculating the Inductor Value

Typically the inductor is set for a ripple current (ΔI_L) of 10% to 35% of the maximum DC load. Regulators requiring fast transient response use a value on the high side of this range, while regulators that require very low output ripple and/or use high-ESR capacitors restrict allowable ripple current:

$$\Delta I_L = \frac{V_{OUT} \bullet (1 - D)}{L \bullet f} \quad (5)$$

where f is the oscillator frequency and:

$$L = \frac{V_{OUT} \bullet (1 - D)}{\Delta I_L \bullet f} \quad (6)$$

Setting the Ramp Resistor Value

The internal ramp voltage excursion (ΔV_{RAMP}) during t_{ON} should be set to 0.6V. R_{RAMP} is approximately:

$$R_{RAMP(K\Omega)} = \frac{(V_{IN} - 1.8) \bullet V_{OUT}}{18x10^{-6} \bullet V_{IN} \bullet f} - 2 \quad (7)$$

where frequency (f) is expressed in KHz.

Setting the Current Limit

The FAN2106 uses its internal low-side MOSFET for current-sensing. The current-limit threshold voltage (V_{ILIM}) is compared to a scaled version of the voltage drop across the low-side MOSFET, sampled at the end of each PWM off-time/cycle.

The default threshold (I_{LIM} open) is temperature compensated.

The 10µA current sourced from the ILIM pin can be used to establish a lower, temperature–dependent, current-limit threshold by connecting an external resistor (R_{ILIM}) to AGND:

$$R_{ILIM(K\Omega)} = 0.45 \bullet R_{DS} \bullet K_T \bullet (I_{OUT} - \frac{\Delta I_L}{2}) + 142.5 \quad (8)$$

where:

I = desired current limit set point in Amps,

R_{DS} is expressed in mΩ,

K_T = the normalized temperature coefficient of the low-side MOSFET (Q2) from Figure 8.

After 16 consecutive, pulse-by-pulse, current-limit cycles, the fault latch is set and the regulator shuts down. Cycling V_{CC} or EN restores operation after a normal soft-start cycle *(refer to Auto-Restart section)*.

The over-current protection fault latch is active during the soft-start cycle.

In case R_{ILIM} is not connected, the IC uses internal default current limit threshold.

Loop Compensation

The loop is compensated using a feedback network around the error amplifier. Figure 22 shows a complete Type-3 compensation network. For Type-2 compensation, eliminate R3 and C3.

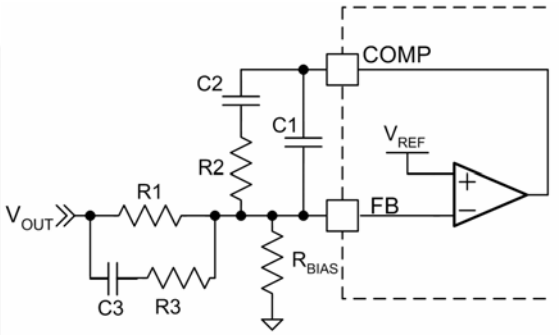

Figure 22. Compensation Network

Since the FAN2106 employs summing current-mode architecture, Type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, Type-3 compensation may be required. The AN-6033 spreadsheet calculator can be used to calculate these component values.

Protection

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, under-voltage, and over-temperature conditions.

An internal “Fault Latch” is set for any fault intended to shut down the IC. When the fault latch is set, the IC discharges V_{OUT} by enhancing the low-side MOSFET until FB<0.25V. The MOSFET is not turned on again unless FB>0.5V. This behavior discharges the output without causing undershoot (negative output voltage).

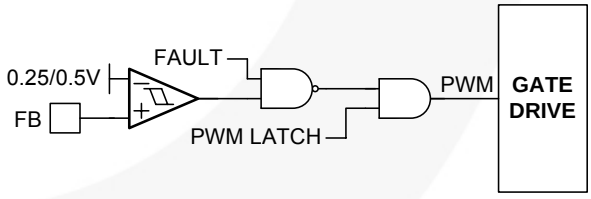

Figure 23. Latched Fault Response

Under-Voltage Shutdown

If voltage on the FB pin remains below the under-voltage threshold for 16 consecutive clock cycles, the fault latch is set and the converter shuts down. This protection is not active until the internal SS ramp reaches 1.0V during soft start.

Over-Voltage Protection / Shutdown

If voltage on the FB pin exceeds the over-voltage threshold for two consecutive clock cycles, the fault latch is set and shutdown occurs.

A shorted high-side MOSFET condition is detected when SW voltage exceeds ~0.7V while the low-side MOSFET is fully enhanced. The fault latch is set immediately upon detection.

The two fault protection circuits above are active all the time, including during soft-start.

Auto-Restart

After a fault, EN pin is discharged by a 1µA current sink to a 1.1V threshold before the 800KΩ pull-up is restored. A new soft-start cycle begins when EN charges above 1.35V.

Depending on the external circuit, the FAN2106 can be configured to remain latched-off or to automatically restart after a fault.

Table 1. Fault / Restart Provisioning

EN pin	Controller / Restart State
Pull to GND	OFF (disabled)
V_{CC}	No restart – latched OFF(After V_{CC} comes up)
Open	Immediate restart after fault
Cap to GND	New soft-start cycle after: t_{DELAY} (ms) = 3.9 • C(nf)

With EN left open, restart is immediate.

If auto-restart is not desired, tie the EN pin to the VCC pin or pull it high after V_{CC} comes up with a logic gate to keep the 1µA current sink from discharging EN to 1.1V.

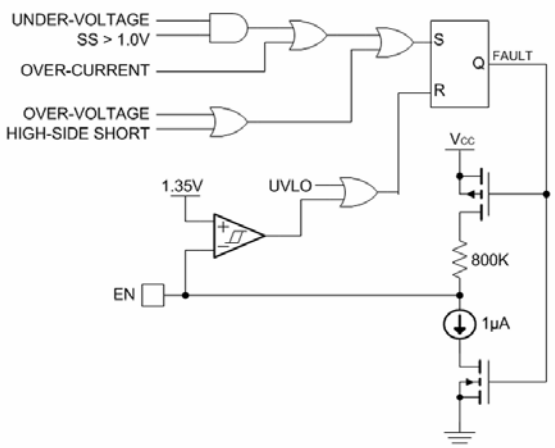

Figure 24. Fault Latch with Delayed Auto-Restart

Over-Temperature Protection

The chip incorporates an over-temperature protection circuit that sets the fault latch when a die temperature of about 150°C is reached. The IC restarts when the die temperature falls below 125°C.

Power Good (PGOOD) Signal

PGOOD is an open-drain output that asserts LOW when V_{OUT} is out of regulation, as measured at the FB pin. Thresholds are specified in the Electrical specifications section. PGOOD does not assert HIGH until the fault latch is enabled (T1.0).

PCB Layout

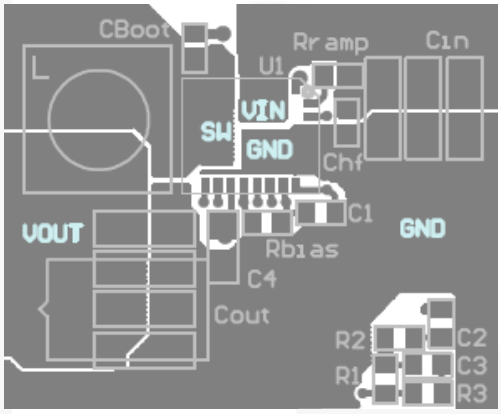

Figure 25. Recommended PCB Layout

Physical Dimensions

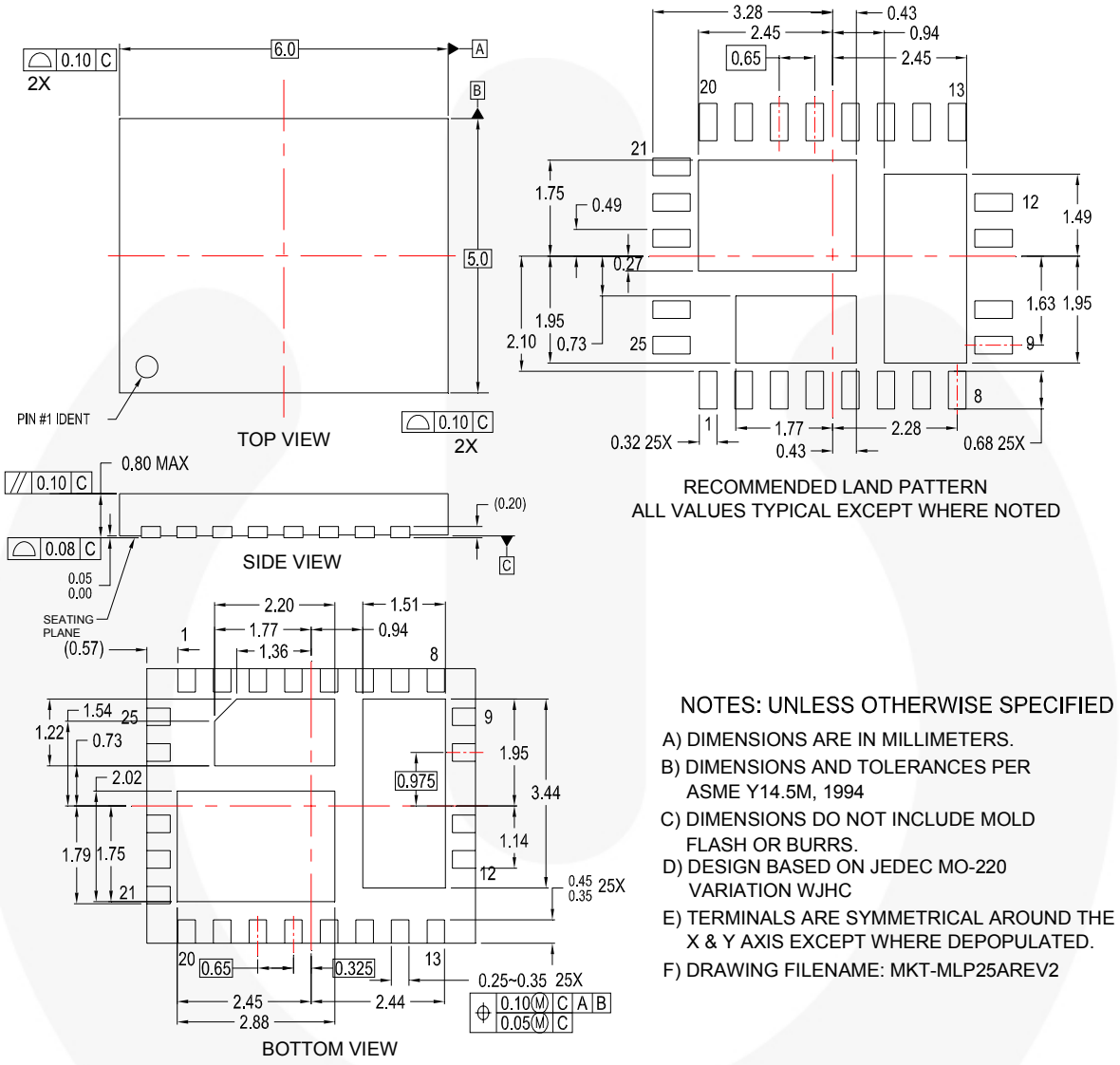

Figure 26. 5x6mm Molded Leadless Package (MLP)

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